VLSI
TECHNOLOGY
VLSI DESIGN FLOW

CURRICULUM

» Introduction to VLSI

- What is VLSI
- VLSI Design Flow
- ASIC
- SoC

SECTION A:

» Fundamentals of Digital Design

FUNDAMENTALS

- Basic Digital Circuits
- Logic gates & Boolean Algebra
- Number System
- Digital Logic Families

» Combinational Logic Design

- Multiplexers
- MUX based design for digital circuits
- Demultiplexers/Decoders
- Adders/Sub tractors
- BCD Arithmetic & ALU
- Comparators & Parity Generator
- Code Converters/Encoders
- Decoders
- Multipliers/Divider

» Sequential Logic Design Priciples

- Bistable Elements,
- Latches and Flip-Flops
- Counters and its application
- Synchronous Design Methodology
- Impediments to Synchronous Design
- Shift Registers
- Design Examples & Case studies

SECTION B:
» Advanced Digital Design

- Synchronous/Asynchronous Sequential Circuits
- ASM charts
- Finite state machine
- Mealy and Moore machine
- State reduction technique
- Sequence Detectors
- Clock Dividers
- Synchronizers & Arbiters
- FIFO & Pipelining

Section C:
» VHDL

- **VHDL OVERVIEW AND CONCEPTS:** Types, object classes, design units, compilation elaboration.
- **BASIC LANGUAGE ELEMENTS:** Lexical elements, syntax, operators, types and subtypes (scalar, physical, real, composite (arrays, records),access files).
- **CONTROL STRUCTURES:** Control Structures and rules (if, case, loop).
- **DRIVERS:** Resolution function, drivers (definition, initialization, creation), ports
- **TIMING:** Signal attributes. “wait” statement, delta time, simulation engine, modeling with delta time delays, VITAL tables, inertial / transport delay
- **ELEMENTS OF ENTITY/ARCHITECTURE:** Entity, architecture, (process, concurrent signal assignment, component instantiation and port association rules, concurrent procedure, generate, concurrent assertion, block, guarded signal).
- **SUBPROGRAMS:** Rules and guidelines (unconstrained arrays. interface class, initialization, implicit signal attributes, drivers, signal characteristics in procedure calls, sides effects),overloading, functions (resolution function, operator overloading, function(resolution function, operator overloading), concurrent procedure.
- **PACKAGES:** Declaration., body, deferred Constant, “use” Clause, Signals, resolution function, subprograms, converting typed objects to strings, TEXTIO, printing objects, linear feedback shift register, random number generation compilation order
- **USER DEFINED ATTRIBUTES, SPECIFICATIONS, AND CONFIGURATIONS:** Attribute declarations, attributes specifications, configuration specification and binding, configuration declaration and binding, configuration of generate statements.
- **DESIGN FOR SYNTHESIS**
  - Constructs, register interface,
  - combinational logic interface, state machine and
  - design styles, arithmetic operations.
- **FUNCTIONAL MODELS AND TESTBENCHES :**
  - Test
  - bench design methodology, BFM Modeling,scenario
  - generation schemes, waveform generator, client/server,
  - text command file, binary command file.

» MINOR PROJECT
Lab Sessions on ModelSIM

SECTION C:
VERILOG

- **Overview of Digital Design with Verilog® HDL**
  Evolution of CAD, emergence of HDLs, typical HDL-based
  design flow, why Verilog HDL?, trends in HDLs.
- **Hierarchical Modeling Concepts**
  Top-down and bottom-up design methodology, differences between modules and module instances,parts of a simulation, design block, stimulus block.
- **Basic Concepts**
  Lexical conventions, data types, system tasks, compiler directives.
- **Modules and Ports**
  Modules definition, port declaration, connecting ports, hierarchical name referencing.
- **Gate-Level Modeling**
  Modeling using basic Verilog gate primitives, description of and/or and Buf/not type gates, rise, fall and turn-off delays, min, max and typical delays.
- **Dataflow Modeling**
  Continuous assignments, delay specification, expressions, operators, operands, operator types.
- **Behavioral Modeling**
  Structured procedures, initial and always, blocking and nonblocking statements, delay control, generate statement, event control, conditional statements, multiway branching, loops, sequential and parallel blocks.
- **Tasks and Functions**
  Differences between tasks and functions, declaration, invocation, automatic tasks and functions.
- **Useful Modeling Techniques**
  Procedural continuous assignments, overriding parameters, conditional compilation and execution, useful system tasks.

» Advanced Verilog Topics

- **Timing and Delays**
  Distributed, lumped and pin-to-pin delays, specify blocks, parallel and full connection, timing checks, delay back-annotation.
- **Switch-Level Modeling**
  MOS and CMOS Switches, bidirectional switches, modeling of power and ground, resistive switches, delay specification on switches.
- **User-Deined Primitives**
  Parts of UDP, UDP rules, combinational UDPs, sequential UDPs Shorthand symbols.
- **Logic Synthesis with Verilog HDL**
  Introduction to logic synthesis, impact of logic synthesis, Verilog HDL constructs and operators for logic synthesis, synthesis design flow, verification of synthesized circuits, modeling tips, design partitioning.
- **Advanced Verification Techniques**
  Introduction to a simple verification flow, architectural modeling, test vectors/testbenches,simulation acceleration emulation, analysis/coverage, assertion checking, formal verification, semi-formal verification, equivalence checking.

System Verilog

- 1) Introduction to system verilog
- 2) Data types:-
  - Integer data type
  - Real and short real
  - Void data types
  - Strings
  - Event
  - User defined
  - Data declaration- Constant variables net reg logic signal aliasing
  - Enumerations
  - Structure and Union
  - Classes
  - Casting
- 3) Arrays
  - Packed and unpacked
  - Dynamic arrays
  - Queues
- 4) Operators and Expressions
  - Arithmetic
  - Logical
  - Operator Loading
  - Conditional
- 5) Procedural statements and Control flow
  - Blocking and non blocking assignments
  - Selection Statements
  - Loops
  - jump
  - Final block
  - Named block
  - Event control
  - Level sensitive seq. control
- 6) Task and functions
  - Argument passing
  - Import and export functions
- 7) Classes
  - Intro
  - Object and its properties and methods
  - Constructor
  - Inheritances
  - Sub classes
  - Overridden members
  - Super class
  - Casting
  - Data hiding and encapsulation
  - Constant class and virtual methods
  - Polymirphism
- 8) Assertions
  - Immediate assertion
  - Concurrent assertion overview

- Boolean exp
- Seq.
- Sequence operation
- Manipulating data in sequence
- Calling sub routines on the match of sequence

LEVEL 2:

» Introduction to ASIC DESIGN METHODOLOGY

- Typical Design Flow
- Specification and RTL Coding
- Statics Timing Analysis
- Placement Routing and Verification
- Step up and hold time
- Delay calculation
- Memory design
- JTAG

» PROJECTS

List of Projects

- Microcontroller Design
- RISC & CISC Processor Design
- I2C,AMBA,Wishbone
- JTAG: Boundary SCAN
- Security control system
- Automated car parking system
- Home control system
- Digital Game